Optimized Design of Low-power Adiabatic Dynamic CMOS Logic Digital PWM using Clock Cut-off Circuit and Miniaturization for SSL Dimming System

Seung-Il Cho, Kodai Aoyama, Naoki Sawada, Mitsuru Mizunuma, Michio Yokoyama
Department of Bio-systems Engineering,
Graduate School of Science and Engineering, Yamagata University
cho_si@ yz.yamagata-u.ac.jp, yoko@yz.yamagata-u.ac.jp

Abstract

In this paper, the low-power adiabatic dynamic CMOS logic (ADCL) digital pulse width modulation (PWM) has been designed for solid state lighting (SSL) dimming system. Architecture of ADCL digital 3-bit PWM is miniaturized. 60 transistors and 15 capacitors were reduced. Furthermore, the clock cut-off circuit which controls wake-up and sleep mode of ADCL D-FFs is proposed. The power consumption of optimized ADCL digital PWM for all bit patterns is found to decrease by 54%.

Keywords: clock cut-off circuit, miniaturization, adiabatic dynamic CMOS logic, digital PWM, SSL dimming system, low-power design

1. Introduction

There is a growing trend toward not using the incandescent lamps because of low-efficiency. Also using the fluorescent lights that have harmful material such as lead and mercury etc, has been reduced by regulation of the heavy metals ; Waste Electrical and Electronic Equipment(WEEE), Restriction of Hazardous Substances(RoHS). As such, development of the solid-state lighting(SSL) that contains light emitting diode(LED), organic light emitting diode(OLED) and polymer light emitting diode(PLED) is expended due to the necessity of new eco-friendly lighting source. And currently, the SSL has formed a broad market from the display to general lighting.

Presently, the SSL system consists of the power part, dimming circuit part and SSL part. Although power consumption of the dimming circuit part is the least, size and power consumption of digital circuit including dimming circuit part will increase for high-performance SSL system in the future. Therefore, low-power design of the dimming circuit part should be needed for low-power SSL system[1-3].

The adiabatic dynamic CMOS logic(ADCL) has been studied to reduce the power loss in conventional CMOS logic for low-power design of logic circuit[3-7]. SSL dimming circuit part was designed using ADCL in Ref. [3]. However, architecture has not been optimized. Furthermore, power consumption occurs by unnecessary operation of ADCL D-FFs in ADCL digital 3-bit pulse width modulation (PWM) at both 0% and 100% of pulse width of PWM output.

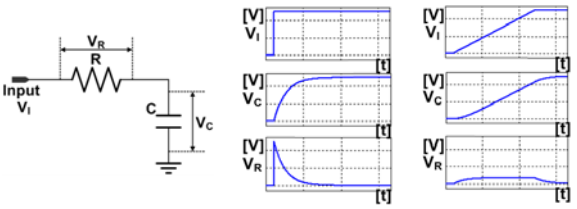
In this paper, the low-power SSL dimming system is designed. ADCL digital 3-bit PWM is miniaturized. Moreover, the clock cut-off circuit which controls wake-up and sleep mode of ADCL D-FFs is proposed.

2. Adiabatic logic

A. Adiabatic Charging

During a sudden transition between high and low levels of input voltage, a load capacitor cannot be charged and discharged immediately. A power dissipation is incurred by resistive component of logic circuit in the conventional CMOS logic, because this logic circuit uses a constant voltage; direct current (DC) power supply. In order to minimize the power dissipation, an adiabatic charging is one of promising candidates with AC power which has slower rising/falling time than charge/discharge time constant[4-5].

Figure 1 shows operations at a normal RC circuit with DC signal and adiabatic charging. Figure 1(b) shows voltage waveforms of DC signal. When voltage is changed from low to high level, the energy dissipation is incurred at the load R until the end of charging at the load C. In this case, current *i(t)*, voltage



(a) RC circuit (b) The DC signal (c) The adiabatic charging

Fig. 1. Operation of a RC circuit

drop of resistance $v_R(t)$ and power dissipation $P_R(t)$ at Fig. 1(a) are

$$i(t) = \frac{V_I}{R} e^{-\frac{t}{CR}}, \quad (1)$$

$$v_R(t) = V_I e^{-\frac{t}{CR}}, \quad (2)$$

$$P_R(t) = \frac{V_I^2}{R} e^{-\frac{2t}{CR}}. \quad (3)$$

On the other hand, Figure 1(c) shows the voltage waveforms of AC signal that has slower rising time than time constant of RC circuit. The energy dissipation is reduced at the load R because of low $v_R(t)$. In this case, $i(t)$, $v_R(t)$, $P_R(t)$ are

$$i(t) = \frac{CV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right)-\left(1-e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right], \quad (4)$$

$$v_R(t) = \frac{RCV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right)-\left(1-e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right], \quad (5)$$

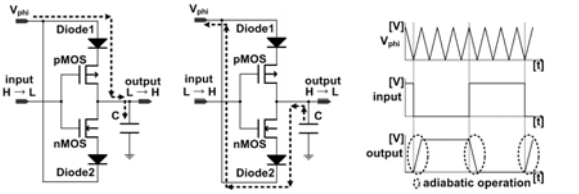
$$P_R(t) = R\left[\frac{CV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right)-\left(1-e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right]\right]^2, \quad (6)$$

where τ is rising time of input and $u(t)$ is unit step function[5, 7].

B. Adiabatic Dynamic CMOS Logic(ADCL)

The ADCL consists of the CMOS logic, AC power and two diodes for the adiabatic charging as it is applied to the CMOS logic. An ADCL inverter gate is shown in Fig. 2. In this circuit, since the output voltage of the ADCL gate is synchronized with the power supply V_{phi}, the operating speed of the ADCL circuits is determined by the frequency of V_{phi}. The principle of ADCL inverter is shown in Fig. 2(a) and (b)[3, 6-7].

When the circuit is operated with the basis on principles (a) and (b), the circuit functions as ADCL inverter. However, if the difference between V_{phi} and



(a) input : H → L (b) input : L → H (c) Operation waveforms

Fig. 2. ADCL inverter and operation waveforms

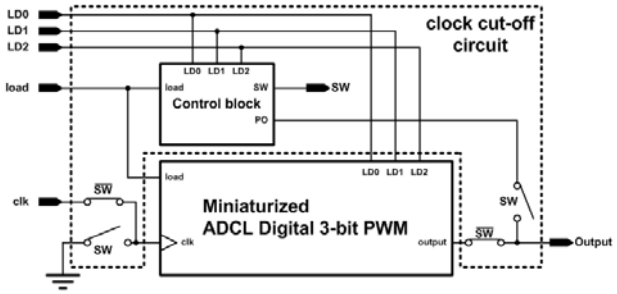


Fig. 3. Proposed low-power ADCL PWM

the voltage across C is large, adiabatic operation will not be established and power will be largely dissipated. Consequently, ADCL inverter works in the adiabatic mode as delineated in Fig 2(c).

The ADCL operates the adiabatic charging whenever logic level of the output is changed from high level to low and conversely. Furthermore, the charge can be reused because the charge reverts to the power source at discharging of load C.

3. Optimized ADCL digital 3-bit PWM

Low-power PWM of SSL dimming system is designed as shown in Fig. 3. First, needless gates at designed ADCL digital 3-bit PWM in Ref. [3] are canceled for miniaturization and low-power consumption of the SSL dimming system. Second, clock cut-off circuit which pauses ADCL D-FFs to occur power consumption by unnecessary operation at both 0% and 100% of pulse width of PWM output is proposed.

A. Miniaturization of ADCL digital 3-bit PWM

In order to miniaturize ADCL digital 3-bit PWM, the block (a) setting PWM pulse width by input-bit is changed from 2 AND gates and OR gate to 3 NAND gates. And the D-FFs to decrease the number of logic gates are used. Comparison of elements is shown in table 1 and miniaturized ADCL digital 3-bit PWM is shown in Fig. 4. 60 transistors and 15 capacitors were reduced.

Table 1. Comparison of elements

	Ref. [3]			This paper		
	No.	Tr.	Cap.	No.	Tr.	Cap.
AND	6	60	12	0	0	0
OR	3	30	6	0	0	0
NAND	0	0	0	9	54	9
D-FF	3	138	24	3	114	18
sum	12	228	42	12	168	27

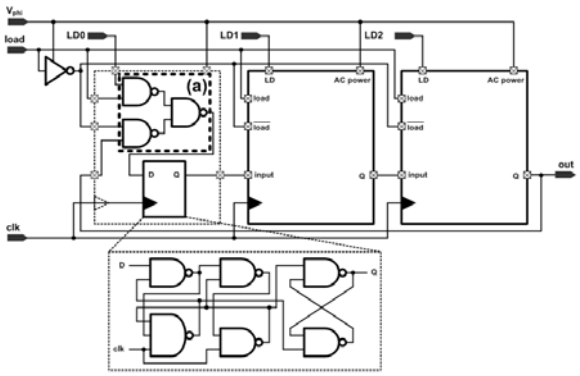


Fig. 4. Miniaturized ADCL digital 3-bit PWM

B. Design of the clock cut-off circuit

Unnecessary operation at both 0% and 100% of pulse width of PWM output occurs power consumption. Designed clock cut-off circuit pauses the D-FFs after cutting off the clock at both input-bit 000(0%) and 111(100%), performs normal operation of the D-FFs at other case.

Figure 5 shows designed control block of clock cut-off circuit. Table 2 shows the truth table of proposed control block. The up-level D-latch is employed to output logic level of the SW and PO by input-bit if the load is reset, on the other hand, to remain logic level of pre-state if the load is set.

4. Simulation results

Optimized ADCL digital 3-bit PWM system is simulated by the PSpice OrCAD 10.3 with 1.2um standard MOS level-3. DC power, AC power and clock are 5V, 33kHz sinewave, 3kHz respectively. The result of simulation is shown in Fig. 6. As a result of simulation, it is conformed that input clock of the

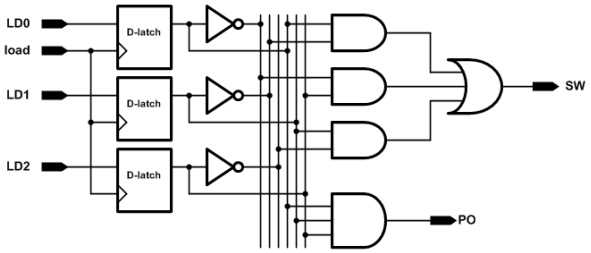


Fig. 5. Control block of clock cut-off circuit

Table 2. The truth table of proposed control block

load	LD0	LD1	LD2	SW	PO
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	1	1	0
1	1	1	1	0	1
0	Don't care	Don't care	Don't care	X_{n-1}	X_{n-1}

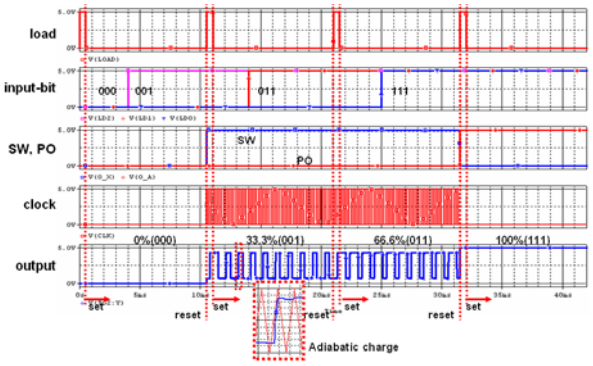


Fig. 6. The result of simulation

ADCL D-FFs is cut off because the SW is high level at both input-bit 000 and 111. Moreover pulse width of PWM output becomes 100% because the PO is high level at input-bit 111.

The power consumption between ADCL digital PWM in Ref. [3] and optimized ADCL digital PWM with proposed clock cut-off circuit in this paper is compared as shown in table 3 and Fig. 7. The power consumption of optimized ADCL digital 3-bit PWM is less than 3nW at both 0% and 100% of pulse width of PWM output. Moreover, the power consumption of optimized ADCL digital PWM for all bit patterns is found to decrease by 54% than that of ADCL PWM of Ref. [3].

Table 3. Comparison of power consumption

[nW]

	000	001	011	111
ADCL Digital PWM [3]	243.5	410.8	351.4	81.9
Miniaturized ADCL Digital PWM	78.0	247.0	246.2	78.0
Optimized ADCL Digital PWM	2.6	245.9	248.2	2.8

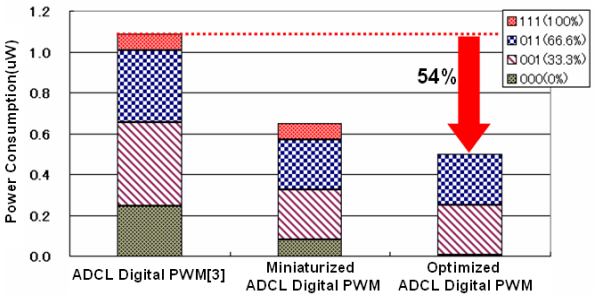


Fig. 7. Comparison of power consumption

5. Conclusion

The optimized low-power ADCL digital PWM has been designed for SSL dimming system. As results of simulation, power consumption of optimized ADCL digital PWM is found to be lower 54% than that of ADCL digital PWM of Ref. [3] because of using the clock cut-off circuit to reduce unnecessary operations and miniaturized ADCL. This result shows the promising usage of optimized ADCL PWM in low-power future SSL dimming system.

References

[1] S. Tarashioon, S.W Koh, W.D van Driel, G.Q. Zhang, "Temperature dependency in performance of solid state lighting drivers," in Proc. Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, pp1-3, April, 2011.

[2] J.Y. Tsao, M.E. Coltrin, Mary H. Crawford, J. A. Simmons, "Solid-State Lighting: An Integrated Human Factors, Technology, and Economic Perspective," Proceeding of the IEEE, vol. 98, no. 7, pp. 1162-1179, July, 2010.

[3] S.-I. Cho and M. Yokoyama "Design of low-power PWM for dimming system of the SSL using Adiabatic Dynamic CMOS Logic," in Proc. 2nd International Symposium on Green Computing and Sustainable Society 2012(GCSS2012), pp. 27-30, Apr. 2012.

[4] A. G. Dickinson and J. S. Dencker, "Adiabatic dynamic logic," IEEE J. Solid-States Circuits., vol. 30, no. 3, pp. 311-315, April 1995.

[5] N. Anuar, Y. Takahashi, and T. Sekine, "4x4-bit array two phase clock adiabatic static CMOS logic multiplier with new XOR," in Proc. IEEE/IFIP VLSI SoC 2010, Sept. 27-29, Madrid, Spain, pp.364-368.

[6] Y. Takahashi, K. Konta, K. Takahashi, K. Shouno, M. Yokoyama, and M. Mizunuma, "Carry propagation free adder/subtracter using adiabatic dynamic CMOS logic circuit technology", IEICE Trans. Fundamentals., vol. E86-A, no. 6, pp.1437.1444, June 2003.

[7] S.-I. Cho, T. Harada, M. Yokoyama "Design of the ultra low-power synchronizer using ADCL buffer for adiabatic logic," IEICE Electronics Express, vol. 9 No. 20, pp1576-1585, Oct. 2012.