Design of Low-power PWM for Dimming System of the SSL using Adiabatic Dynamic CMOS logic

Seung-Il CHO and Michio YOKOYAMA
Department of Bio-system Engineering Yamagata University
tye91221@st.yamagata-u.ac.jp, yoko@yz.yamagata-u.ac.jp

Abstract

In this paper, the low-power consumption design of the pulse width modulation(PWM) circuits have been investigated, which are dimming circuits of the solid state lighting(SSL). The digital 3-bit PWM using adiabatic dynamic CMOS logic(ADCL) is proposed. The power consumption of PWM circuits designed with the conventional CMOS logic and ADCL are compared and evaluated using the computer simulation and implementation. The result of comparison has shown that the power consumption of the digital 3-bit PWM using ADCL is smaller than that using CMOS for dimming circuit of the SSL. In addition, low-power advantage of ADCL is proved with increasing the number of input bits of PWM using simulation.

1. Introduction

Recently, the worldwide interest about several environmental issues has increased. So the green information technology(IT) has attracted attentions for the low-power consumption of electronic equipments, as an example, the interests about development of the smart grid, solar cell system, hybrid electric vehicle are increasing. Also energy-saving and development of eco-friendly technologies are needed for the general lighting system. As such, development of the solid-state lighting(SSL) is expended due to the necessity of new eco-friendly lighting source. The SSL system consists of the power part, dimming circuit part and SSL part. At this system, the pulse width modulation(PWM) is usually used for the dimming circuit[1][2].

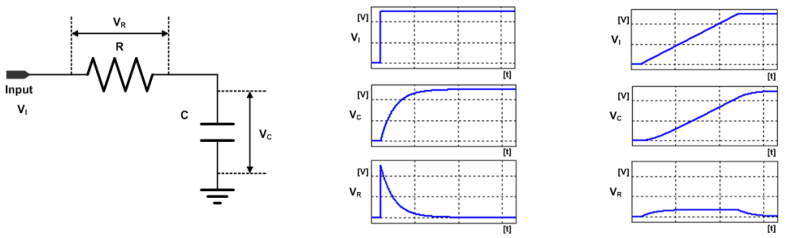
Low-power design of the dimming circuit is needed for low-power SSL system. The adiabatic dynamic CMOS logic(ADCL) has been studying to reduce the power loss in conventional CMOS logic for low power design of logic circuit[3][4]. In this paper PWMs are designed, which is dimming circuit of the SSL using the ADCL for low-power consumption. We also compare power consumption of CMOS and ADCL digital 3-bit PWM. In order to compare power consumption PWMs are simulated with PSpice and implemented on the print circuit board(PCB)s. Furthermore, power consumption of CMOS and ADCL digital 10-bit PWM are compared using simulation.

2. Adiabatic logic

A. Adiabatic charging

During sudden transition, between high and low level of input voltage, the load capacitor cannot be charged and discharged. The power loss is incurred by resistive

component of logic circuit in the conventional CMOS logic circuits, because this logic circuit uses a constant voltage; the direct current(DC) power supply[3][4]. In order to minimize the energy loss, the adiabatic charging is one of promising candidates with the alternate current(AC) power, which has slower rising/falling times than charge/discharge time considering the load capacitor. Fig. 1 shows operations of DC signal and adiabatic charging at the normal RC circuit.



(a) RC circuit (b) the DC signal (c) the adiabatic charging

Fig. 1. Operation of a RC circuit

B. Adiabatic Dynamic CMOS logic(ADCL)

The ADCL consists of the CMOS logic, AC power and two diodes for the adiabatic charging as it is applied to the CMOS logic[5]. The ADCL works like the same logic as the CMOS inverter turning on and off the pMOS and nMOS by following input signal. The ADCL works the adiabatic charging using the AC power of the triangle or sine wave. Furthermore, two diodes maintain the high or low level of output voltage. The ADCL operates the adiabatic charging both the rising and falling of the output, and the charge can be reused.

3. Design of digital 3-bit PWM and the results of simulation

The digital 3-bit PWM for dimming circuit of the SSL and design those using conventional CMOS and ADCL are proposed. We also compare power consumption of ADCL digital 3-bit PWM and that of CMOS digital 3-bit PWM. The digital 3-bit PWM is proposed as shown in the Fig. 2. This output pulse width of PWM can control dimming of SSL.

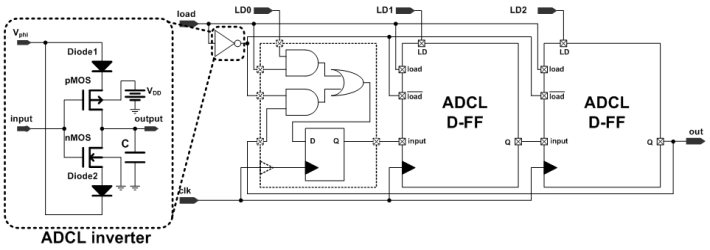


Fig. 2. Digital 3-bit PWM

Designed CMOS and ADCL digital 3-bit PWM are simulated by the PSpice and 1.2um CMOS process. When input bit is 001, the result of simulation of the ADCL digital 3-bit PWM is shown in Fig. 3. The output pulse width of PWM is about 33.3% and characteristics

of ADCL, the adia batic charging are confirmed in Fig. 3. The power consumption between CMOS digital 3-bit PWM and ADCL digital 3-bit PWM is compared as shown in Fig. 4. The power consumption of ADCL digital 3-bit PWM to operate adiabatic charging and charge recycling is lower than that of CMOS at all input bit.

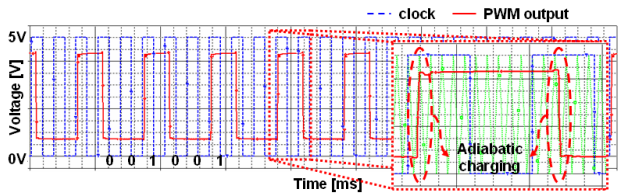


Fig. 3. The result of PSpice simulation

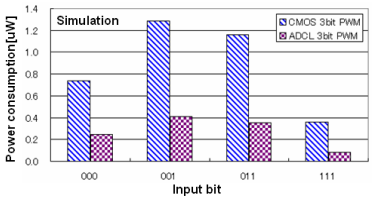
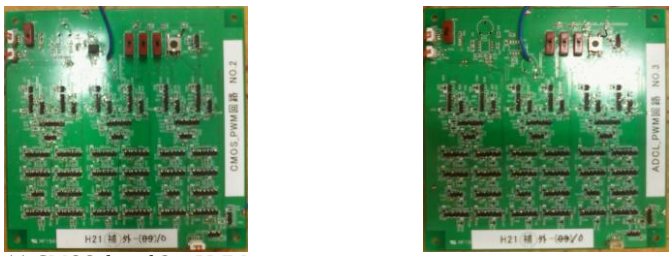


Fig. 4. Comparison of power consumption

4. Implementation and experimental results

In order to measure power consumption of CMOS and ADCL digital 3-bit PWM, those have been fabricated on the print circuit board(PCB)s using 2SK1062(nMOS), 2SJ168(pMOS), 1SS400(diode) and load capacitor 1000pF. And the size of PCB is 15cm X 15cm as shown in Fig. 5.



(a) CMOS digital 3-it PWM (b) ADCL digital 3-bit PWM

Fig. 5. PCBs of digital 3bit PWM

DC power, AC power and clock are 10V, 33kHz sinewave, 3kHz respectively. Fig. 6 shows the adiabatic charging operation of ADCL. The measured power consumption of implemented PCBs is compared as shown in Fig. 7. The measured result is same trend with the simulation result. Furthermore the measured power consumption of ADCL digital 3-bit PWM is much lower than that of CMOS at all input bit.

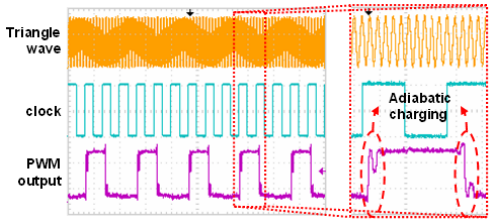


Fig. 6. The result of measurement

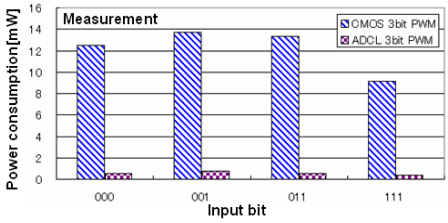


Fig. 7. Comparison of power consumption

In addition, it is simulated by the PSpice to increase the number of input bits of PWM. As shown in Fig. 8, we confirmed that the more the number of input bits or the logic gates increases, the more the gap of power consumption of CMOS and ADCL increases. Hence, low-power advantage of ADCL is found to be larger than that of CMOS, especially with increasing multi-bit.

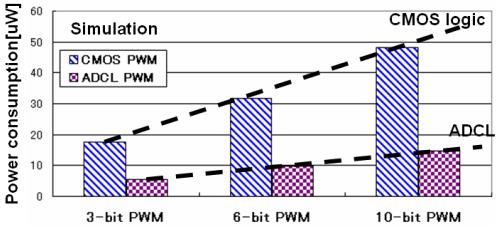


Fig. 8. Comparison of power consumption

5. Conclusion

In this paper, we have designed the low-power consumption of digital 3-bit PWMs which are dimming circuits of the SSL. Simulation and experiment are conducted to confirm operation of proposed digital 3-bit PWM using ADCL and CMOS and those power consumptions are compared. In the result of comparison, the power consumption of ADCL digital 3-bit PWM was found to be lower than those of CMOS.

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