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Design of the ultra low-power synchronizer using ADCL buffer for adiabatic logic

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Abstract: The adiabatic dynamic CMOS logic (ADCL) has been studied to reduce the power dissipation in conventional CMOS logic. The clock signal of logic circuits should be synchronized with the AC power source to maintain adiabatic charging/discharging with low power for the ADCL. In this paper, an ultra low-power synchronizer using ADCL buffer is proposed. The ADCL buffer has been designed using features of automatic synchronization between AC signal and output of gate stage. Power consumptions of the proposed ADCL synchronizer are found to be 99.4 nW at best case and 109.8 nW at worst case, when AC signal and clock frequencies are 110 MHz and 10 MHz, respectively.

Keywords: synchronization, adiabatic dynamic CMOS logic (ADCL), low power, ADCL buffer

Classification: Integrated circuits

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1 Introduction

Low-voltage, low-power, and highly integrated circuits (IC) are always the trends for IC design, especially for portable devices such as personal digital assistant (PDA), smart phone, and tablet PC, etc. due to the limitation of battery capacity. Moreover, a demand for high rate data communication (HRD) is driven by growing popularity of consumer products. Therefore, a lot of studies have been performed for high integration and low-power consumption.

The adiabatic logics have been studied to reduce the power dissipation in conventional CMOS logic for low power design of logic circuits [1, 2, 3, 4]. In particular, the adiabatic dynamic CMOS logic circuit (ADCL) achieves ultra low energy dissipation by restricting current flow across devices with low voltage drop and by recycling the energy stored on load capacitors. It is known that output signal of the ADCL gates is synchronized with alternate current (AC) power supply [5, 6, 7].

A synchronous circuit is needed for adiabatic charging when an AC power supply and a clock generator are respectively designed. The conventional phase locked loop (PLL) and delay locked loop (DLL) are usually used for synchronization of signals. However, the conventional PLL and DLL have a problem of large power consumption [8, 9, 10, 11, 12]. Hence, the power part of ADCL should be designed to have both synchronization and low-power operation for the ADCL system.

In this paper, an ultra low-power synchronizer for ADCL system is proposed. The proposed circuit synchronizes between AC signal and clock sig-

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nal using the ADCL buffer. Furthermore, simulation results have shown that power consumption of this synchronizer is less than that of conventional PLL and DLL.

The rest of this paper is organized as follows. In section 2 the adiabatic charging; standard operation of adiabatic logic is described, then the ADCL system and its power part are described. An ultra low-power synchronizer is designed using ADCL buffer in section 3. Section 4 gives simulation results of designed circuits using a 0.18 μm standard CMOS technology. Finally, section 5 concludes the paper.

2 Adiabatic logic

2.1 Adiabatic charging

During a sudden transition between high and low levels of input voltage, a load capacitor cannot be charged and discharged immediately. A power dissipation is incurred by resistive component of logic circuit in the conventional CMOS logic, because this logic circuit uses a constant voltage; direct current (DC) power supply. In order to minimize the power dissipation, an adiabatic charging is one of promising candidates with AC power which has slower rising/falling time than charge/discharge time constant [1, 2, 3].

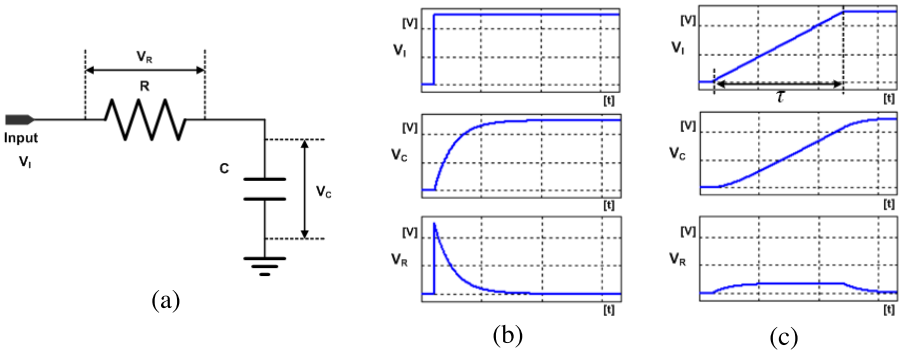

Fig. 1. (a) RC circuit, (b) DC signal, (c) Adiabatic charging

Figure 1 shows operations at a normal RC circuit with DC signal and adiabatic charging. Figure 1 (b) shows voltage waveforms of DC signal. When voltage is changed from low to high level, the energy dissipation is incurred at the load R until the end of charging at the load C. In this case, current $i(t)$, voltage drop of resistance $v_R(t)$ and power dissipation $P_R(t)$ at Fig. 1 (a) are

$$i(t) = \frac{V_I}{R} e^{-\frac{t}{CR}}, \tag{1}$$

$$v_R(t) = V_I e^{-\frac{t}{CR}}, \tag{2}$$

$$P_R(t) = \frac{V_I^2}{R} e^{-\frac{2t}{CR}}. \tag{3}$$

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On the other hand, Figure 1 (c) shows the voltage waveforms of AC signal that has slower rising time than time constant of RC circuit. The energy dissipation is reduced at the load R because of low $v_R(t)$. In this case, $i(t)$, $v_R(t)$, $P_R(t)$ are

$$i(t) = \frac{CV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right)-\left(1-e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right], \tag{4}$$

$$v_R(t) = \frac{RCV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right)-\left(1-e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right], \tag{5}$$

$$P_R(t) = R\left[\frac{CV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right)-\left(1-e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right]\right]^2, \tag{6}$$

where τ is rising time of input and $u(t)$ is unit step function [4].

2.2 Adiabatic dynamic CMOS logic (ADCL)

The ADCL circuits consist of CMOS logic, AC power and two diodes to keep high and low levels [5, 6]. An ADCL inverter gate is shown in Fig. 2 (a). In this circuit, since the output voltage of ADCL gate is synchronized with power supply V_{phi}, operating speed of the ADCL circuits is determined by frequency of V_{phi}. The principle of ADCL inverter is shown in Figures 2 (b) and 2 (c).

Principle (I) input: High → Low
In Figure 2 (b), pMOS and nMOS are ON and OFF, respectively. In this case, supply current path is generated and the load capacitor C is adiabatically charged by V_{phi}. Then high level is kept with diode1.

Principle (II) input: Low → High
In this condition, conversely, pMOS and nMOS are OFF and ON, respec-

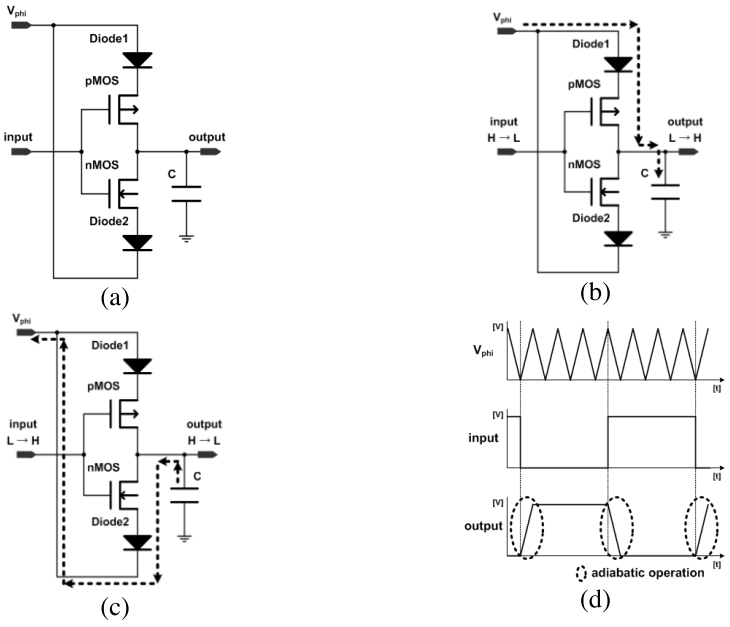

Fig. 2. (a) ADCL inverter, (b) input: H → L, (c) input: L → H, (d) Operation waveforms

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tively. In this case the current path is generated as shown in Fig. 2 (c) and the charge in C is adiabatically discharged into V_{phi}.

If the difference between V_{phi} and the voltage across C is large, adiabatic operation will not be established and power will be largely dissipated. Consequently, ADCL inverter works in the adiabatic mode as delineated in Fig. 2 (d).

In addition to adiabatic charging, charge reuse is also effective to low power consumption in ADCL. The charge can be reused because the charge reverts to the power source at discharging of load C. On the other hand, the output voltage is delayed by 0.5 peried of V_{phi} per gate in the ADCL circuit. Also, AC power supply and input (or clock) signal should be synchronized.

2.3 Power source of ADCL system

Figure 3 shows the synchronized and unsynchronized waveforms of AC power supply, clock and output signal. If the clock signal is unsynchronized with AC power supply, non-adiabatic operation is given at the output. This leads to higher power consumption as indicated in Figures 3 (b) and 3 (c).

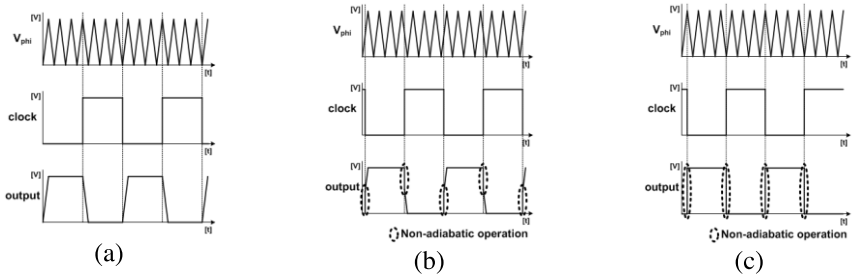

Fig. 3. (a) Synchronized waveforms (phase diff. 180°), (b) Unsynchronized waveforms (phase diff. 270°), (c) Unsynchronized waveforms (phase diff. 0°)

Therefore, a synchronous circuit is needed for adiabatic charging when an AC power supply and a clock generator are individually designed as shown in Fig. 4.

Conventional PLL and DLL are used for the synchronization of signals. However, the power consumptions of them are very large; dozens of mW [8, 9, 10, 11, 12]. Hence, The power source which has both synchronization and low-power consumption should be used for the ADCL system.

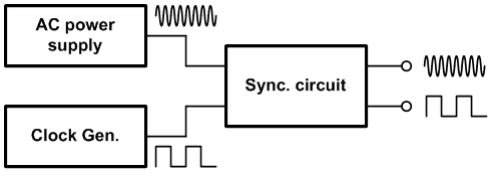

Fig. 4. The power source using a synchronizer for ADCL

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3 Design of ultra low-power synchronizer using ADCL buffer

As explained in section 2, the ADCL has features; i) charge/discharge of load capacitor and hold of levels are set by switching MOS and diode connection MOS, ii) output waveform is tend to follow rising/falling of AC signal at change. Here, synchronization of multi-stage ADCL block is considered. Though clock signal is not synchronized with AC power supply, output signals after the stage 3 are automatically synchronized with AC power supply because of above features. In this case, ADCL blocks from stage 1 to stage 3 cannot operate for low-power consumption because of unsynchronization. In ADCL system, the more blocks using input clock increase, the higher power is consumed. Hence the synchronization between AC signal and clock signal should be needed in the power part for low-power consumption in order not to input non-synchronized signals into ADCL system.

In this section, an ultra low-power synchronizer is proposed using the ADCL buffer as shown in Fig. 5. Used MOS library is a 0.18 μm standard CMOS Technology. The MOS size W/L is 0.22 μm/0.18 μm for all transistors and load capacitor size is 1 pF and 0.01 fF at 33 kHz and 110 MHz of V_{phi} frequency respectively.

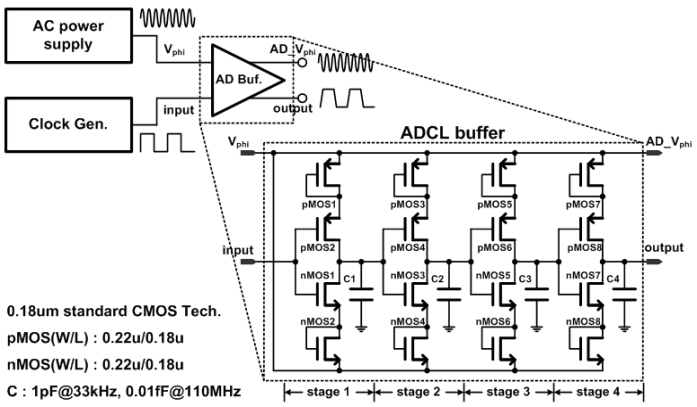

Fig. 5. Proposed ultra low-power synchronizer for ADCL system

Certainly, output signals of not only stage 4 but stage more than 4 are automatically synchronized with AC power supply. Because 4-stage ADCL buffer has the least power consumption, 4-stage ADCL buffer is designed as synchronizer of ADCL system.

Figure 6 shows output waveforms of synchronized (a) and non-synchronized (b), (c), (d) in 4-stage ADCL buffer. Though clock signal is not synchronized with AC power supply at stage 1, output signal of stage 4 is automatically synchronized with AC power supply.

4 Simulation results and evaluation

The proposed ultra low-power synchronizer using ADCL buffer has been simulated using hspice with a 0.18 μm standard CMOS technology.

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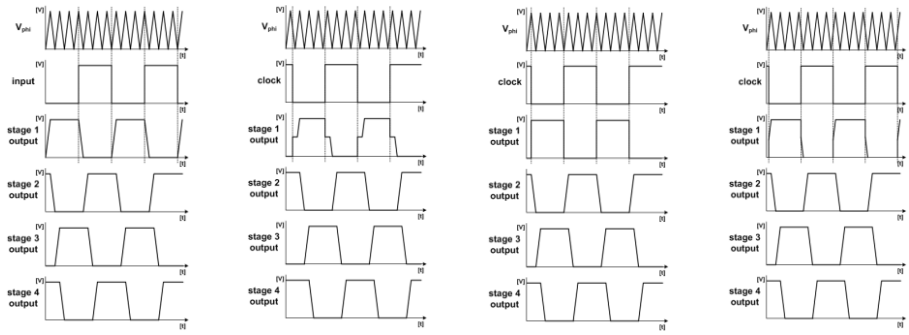

Fig. 6. Output waveforms of the proposed synchronizer (a) phase diff. 180°, (b) 270°, (c) 0°, (d) 90°

Figure 7 shows the results of simulation. The operation of designed synchronizer has been confirmed by simulation. Furthermore, the clock signal was confirmed for the adiabatic charging and synchronized with AC power signal in Figures 7 (c) and 7(d).

Table I. Power consumptions of the proposed synchronizer for ADCL system

AC freq. [Hz]	Clock freq. [Hz]	Power supply [V]	Phase diff. [°]	Power con. [nW]
33k	3k	1.8	180(best case)	16.59
			270	16.64
			0(worst case)	19.80
			90	16.66
110M	10M	1.8	180(best case)	99.4
			270	100.8
			0(worst case)	109.8
			90	101.0

Table I shows power consumptions of the proposed synchronizer for ADCL system. The power consumptions of the proposed synchronizer are 16.59 nW at best case and 19.80 nW at worst case, when AC signal is 33 kHz and clock was 3 kHz. Moreover those are 99.4 nW at best case and 109.8 nW at worst case, when AC signal is 110 MHz and clock was 10 MHz.

In order to confirm operation of total ADCL system, the proposed synchronizer and ADCL 3-bit PWM of Ref. [5] have been simulated using hspice with a 0.18 μm standard CMOS technology. Operation of the proposed synchronizer and ADCL system has been confirmed as shown in Fig. 8.

The power consumption of proposed ultra low-power synchronizer using ADCL buffer is compared with that of conventional synchronous circuits [8, 9, 10, 11, 12]. Table II summarizes several specifications of synchronous circuits. It shows that the power consumption of proposed ADCL synchronizer is lower than that of [12]; 16 mW. Therefore, the proposed synchronizer using ADCL buffer has been found to consume lower power than the others.

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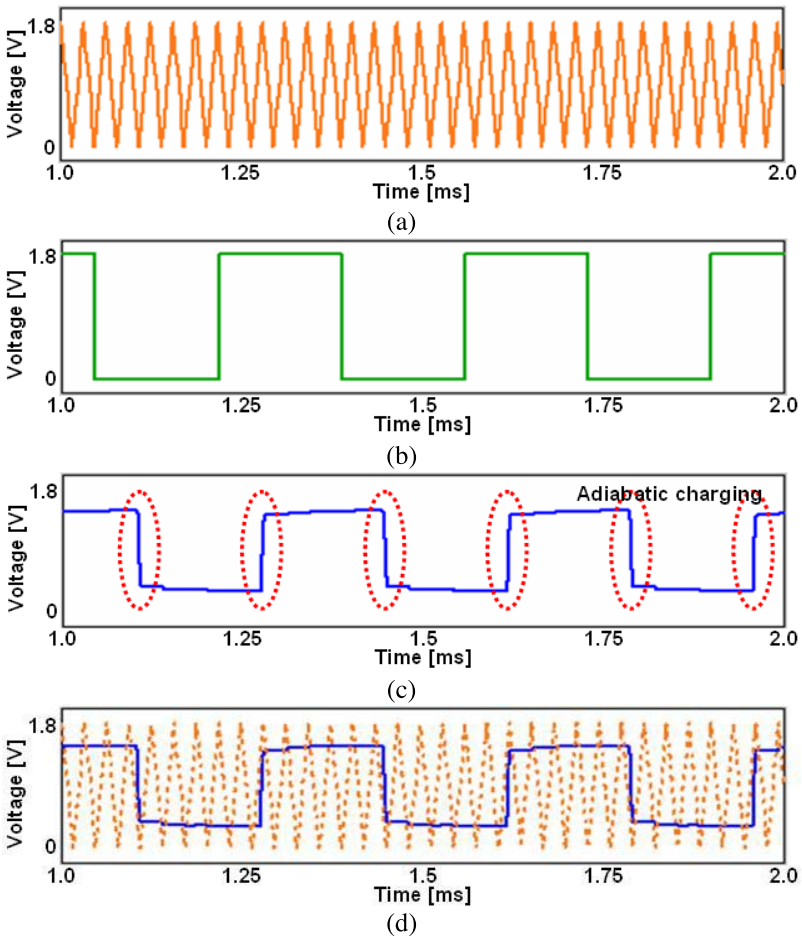

Fig. 7. Output waveforms (a) AC power supply, (b) clock Gen., (c) the proposed synchronizer, (d) An overlap between (a) and (c)

Table II. Comparison of power consumptions

Paper	Process	Power supply [V]	Freq.[Hz]	Power con.	Issue date
[8]	0.18um	1.8	133M	53mW	Apr. 2009.
[9]	0.18um	1.8	800M ~ 1.6GHz	17mW@1.6GHz	Oct. 2009.
[10]	0.13um	1.2	120M ~ 2G	21mW@2GHz	Nov. 2009.
[11]	0.18um	1.8	120M ~ 2.16G	16.2mW@2.16GHz	Apr. 2011.
[12]	0.18um	1.8	100M ~ 1G	16mW@100MHz 64mW@1GHz	Aug. 2011.
This work	0.18um	1.8	AC : 33k Clock : 3k	Worst : 19.80nW Best : 16.59nW	
			AC : 110M Clock : 10M	Worst : 109.8nW Best : 99.4nW	

In the reference [5], power consumption of the ADCL digital PWM has been reduced to 30% of that of CMOS digital PWM. In the total system, an AC power supply and a synchronizer as well as a clock generator should be needed to operate adiabatic charging with low power for ADCL system,

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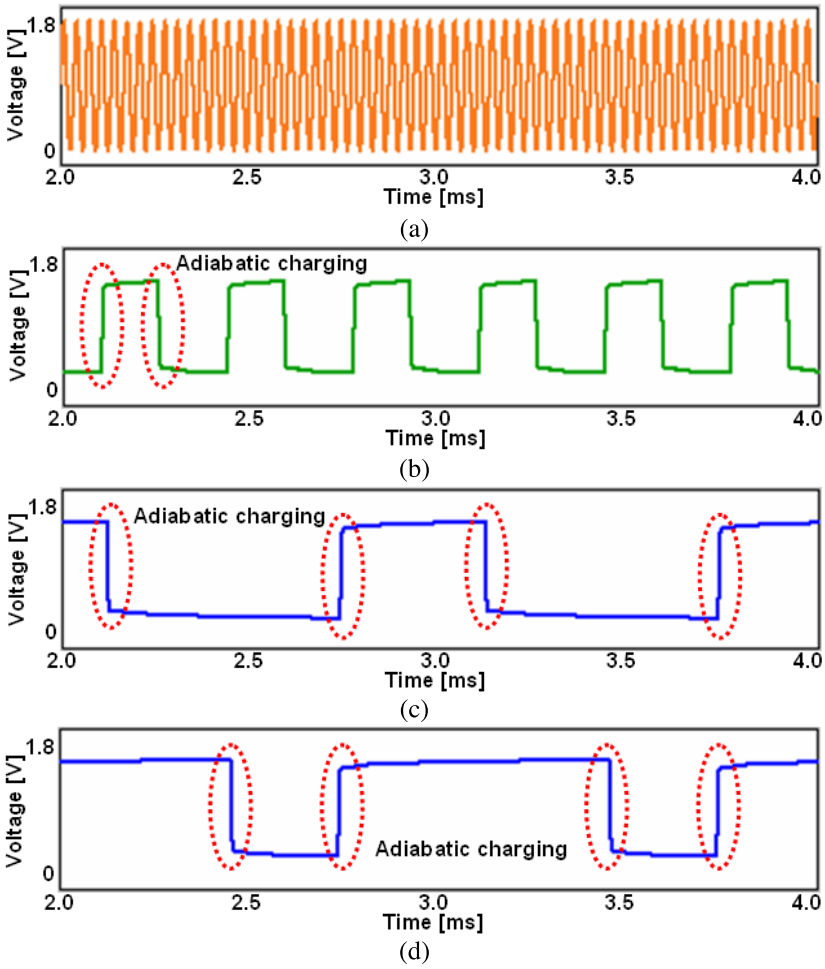

Fig. 8. Output waveforms (a) OSC core, (b) the proposed synchronizer using ADCL buffer, (c) ADCL 3-bit PWM (input bit 100), (d) ADCL 3-bit PWM (input bit 110)

while only a clock generator is needed for CMOS logic system. Because of that reason, power consumption of ADCL system that has a large power AC supply and synchronizer doesn't become lower than that of CMOS system, although power consumption has been reduce to 30% at the logic block parts. However, power consumption of the proposed synchronizer only for ADCL in this paper is extremely low at both best case and worst case. Design of the low-power ADCL system will be realized when the proposed ultra low-power synchronizer is used.

5 Conclusion

A novel ultra low-power synchronizer circuit for ADCL system has been proposed using the designed ADCL buffer. The power consumptions of proposed ADCL synchronizer are 16.59 nW at best case and 19.80 nW at worst case, when AC signal is 33 kHz and clock is 3 kHz. Moreover those are 99.4 nW at best case and 109.8 nW at worst case, when AC signal is 110 MHz and clock is 10 MHz. The proposed ADCL synchronizer was found to have less power

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consumption than conventional synchronous circuits.

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